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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,665	07/21/2003	Lawrence C. West	107262.199US1 and 7090/P0	5061

7590 01/23/2006

PATENT COUNSEL, Legal Affairs Dept.
Applied Materials, Inc.
Box 450A
Santa Clara, CA 95052

EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,665	WEST ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,34,35 and 48-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,34,35 and 48-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/5/03;2/9/04;*. 12/16/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The replacement drawings were received on 10/20/05. These drawings are approved.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 32, 34, 35, 48-53, 55, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,196 to Noble in view of U.S. Patent Publication No. 2002/0146864 to Hoel and U.S. Patent No. 5,098,861 to Blackstone.

Regarding claims 32, 35, 48, and 51-53, Noble discloses a method of producing an optical ready substrate comprising: providing a carrier substrate (14, 74) made of silicon (column 3, lines 1-5) and having a front (top in figure 1 or 9) and back (bottom of 14) side, by using a first set of fabrication processes (figures 2A-8) fabricating optical signal circuitry (12, 22, 23, 24, 27; alternately 72; column 3, lines 1-10) on the front side of the carrier substrate designed to provide signals to the microelectronic circuitry (through 26 and 28 in figure 1 or directly emitted from waveguide to a surface photodetector in figure 9) to be fabricated at a later time (optical circuit layers 12, 22, 23, 24, 27, and 72 are clearly fabricated prior to the circuitry in the SOI layers 20, 88, since the buried oxide layer and SOI layers completely bury the optical circuit), the

optical signal circuitry made up of semiconductor photonic elements (22, 23, 24, 27, 76, 78) interconnected by an optical waveguide (12, 72) for carrying an optical signal having a wavelength of 850 nm or less (waveguide is PSG – column 3, lines 35-45, which is a silica or silicon dioxide. Hence, the waveguide must inherently be capable of carrying an optical signal of 850 nm or less, as admitted in the Applicant's specification, page 10, lines 16-19), and creating a top surface (20, 88) above the optical signal circuitry that is of sufficient quality to permit the microelectronic circuitry to be fabricated thereon (Noble teaches that transistors and photodetectors - see figures 1 and 9 – are formed in the SOI layer; hence, it must be of "sufficient quality to permit microelectronic circuitry to be fabricated thereon") using a second set of semiconductor fabrication processes (see column 6, lines 12-50).

Noble does not disclose sending the optical ready substrate to a purchaser that will subsequently fabricate the microelectronic circuitry thereon, but rather, uses the same entity for fabricating both the optical signal circuitry and the microelectronic circuitry.

Hoel teaches that it is beneficial to partially fabricate portions of integrated circuits shared among many final integrated circuit designs, store the partially fabricated circuits in inventory, and later customize the circuits using a second set of fabrication processes, in order to improve cost and processing time (see paragraphs 0004 and 0021).

Blackstone teaches that it is known in the art to partially fabricate a semiconductor wafer and then sell the partially fabricated wafer to a semiconductor manufacturer, who then will complete the fabrication process (column 4, lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Noble, such that a second entity performs the microelectronic

circuitry fabrication after purchasing the partially finished substrate, as suggested by Hoel and Blackstone. The rationale is as follows: The method disclosed by Noble is substantially identical to that claimed by the Applicant, except that after the formation of the optical ready substrate taught by Noble (corresponding to the point in the fabrication process at which the SOI layer has been deposited, but the microelectronic circuitry has not yet been formed), the microelectronic circuitry is then fabricated by Noble, rather than by a second entity. Since Hoel and Blackstone both indicate that a second party can advantageously purchase partially fabricated wafers, and thus reduce the cost and time of manufacturing by not needing to perform the first set of processes and not needing to possess any specialized equipment required for such manufacture, it is well within the purview of a person skilled in the art to recognize that the optical-ready substrate of Noble can be sent to a second party for fabricating custom microelectronic circuitry in the SOI layer for the advantages listed supra. Since a person skilled in the art would reasonably expect that transfer of partially fabricated wafers from a first party to a second party would involve a purchase of the fabricated wafer, and since Blackstone indicates that the practice of selling partially fabricated wafers is known in the art, one would reasonably deduce that the second party performing the second set of processes is a "purchaser."

Regarding claim 34, Noble discloses that fabricating the optical signal circuitry may comprise fabricating an optical clock signal distribution network (see column 9, line 57 – column 10, line 35).

Regarding claims 49, 50, 55, and 56, Noble does not indicate the specific methods by which the SOI layer is formed.

Blackstone teaches forming an SOI layer by forming an oxide layer (106) on a second substrate (100), bonding the structure to a front side of a first wafer, and then thinning the second wafer (see Figure 4A; column 4, lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of Blackstone for forming the SOI structure of Noble as modified by Hoel and Blackstone, because Noble is silent as to the exact method of SOI formation, which would lead one having ordinary skill in the art to seek out conventional and well known methods, such as that disclosed by Blackstone, for forming such a structure.

4. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noble in view of Hoel and Blackstone, as applied to claim53 above, and further in view of U.S. Patent No. 5,195,161 to Adar et al.

Noble discloses phosphorus doping in the silica core to control the characteristics of the light transmission of the waveguide (see column 4, line 55 – column 5, line 10).

Noble does not disclose that GeO could be used as a dopant for the core.

Adar discloses that phosphorus, titanium, and germanium are commonly known dopants for silica waveguide cores.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Ge (which is necessarily present as the oxide of Ge, GeO) as the dopant of the silica core of Noble, because Adar shows that GeO and P are art recognized equivalents suitable for doping silica and controlling the light transmission therethrough. It has been held that the

selection of a known material based on its suitability for its intended use is prima facie obvious (see Sinclair & Carroll Col, Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 1945).

Response to Arguments

5. Applicant's arguments filed 10/20/05 have been fully considered but they are not persuasive.

The Applicant argues that Hoel and Blackstone are not particularly applicable to Noble, since Hoel involves processes in which both standard and customized masks are used to form the final circuit, and the masks are for forming vias and metal interconnects, and since Blackstone does not teach wafers to be sold having circuits or devices therein, nor does Blackstone indicate that anything other than a generic wafer is to be sold. The Applicant further argues that there is no motivation to combine Hoel or Blackstone with Noble in the manner proposed by the examiner.

This is not persuasive, because Hoel and Blackstone are not being relied upon to provide any specific structure formed in the second set of processes. The Examiner notes that Noble already teaches a first set of processes for forming the buried optical circuitry and SOI structure, thus resulting in the "optical-ready substrate" claimed by the Applicant, and a second set of processes whereby the microelectronic circuitry is formed in the optical-ready substrate (see column 3, lines 1-27; Noble describes forming the SOI structure such that circuitry "can be formed" thereon). Hence, the only thing missing in Noble is the concept of using a second entity to perform the microelectronic circuitry fabrication. It is highly dubious that a mere change of

entities in the middle of a fabrication process would be sufficient to support patentability over a reference teaching the process in which a single entity performs each fabrication step, since it is the steps performed, and not the identity of the person performing the steps that distinguishes a method over the closest prior art. Nevertheless, Hoel and Blackstone are cited to provide evidence that it is known in the art for a wafer to be partially fabricated by one entity, and then sold to another entity to complete the fabrication. Hence, a combination of Hoel and Blackstone with Noble only changes Noble in that the wafer is sold to a second entity, which then completes the microelectronic circuitry fabrication disclosed by Noble. Since a person skilled in the art would readily recognize that the purchase of a partially formed wafer structure eliminates the need to perform the fabrication steps for forming the underlying layers as well as eliminating the specialized equipment necessary for fabricating the underlying layers (i.e., wafer bonding equipment for forming the SOI structure, growth or regrowth equipment necessary for producing the buried optical waveguide), the concept of selling a partially fabricated structure to a second entity is considered obvious over Hoel and Blackstone.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

LAURA M. SCHILLINGER
PRIMARY EXAMINER

Replacement Drawings
Approved
-JMS
1/19/06

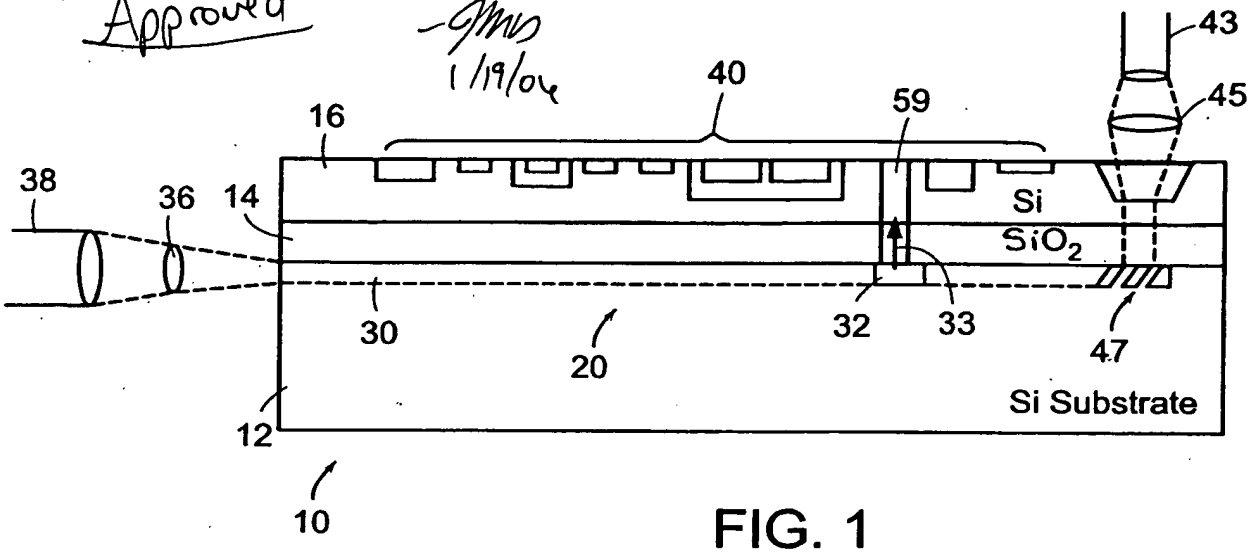

FIG. 1

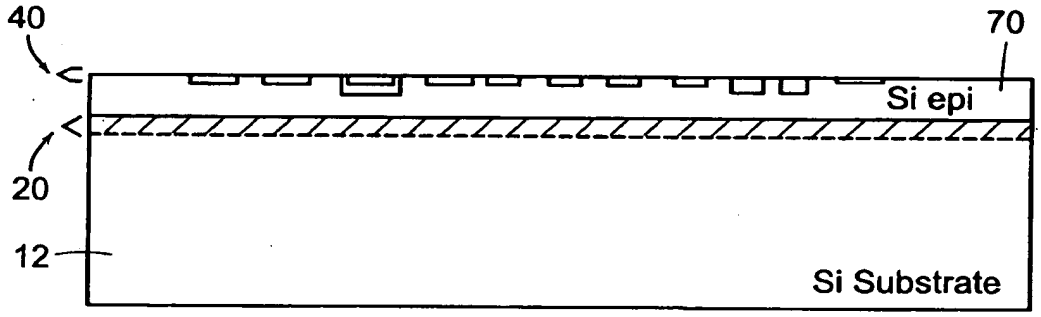

FIG. 2

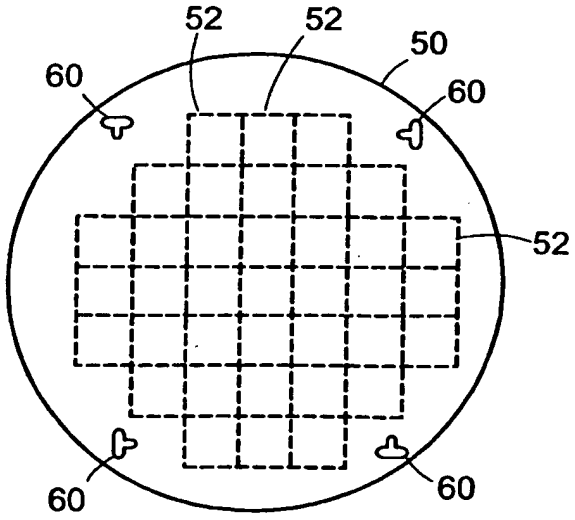

FIG. 3